

REMARKS

This communication is a full and timely response to the aforementioned final Office Action dated March 12, 2010. By this communication, claims 1 and 13-18 are amended, and claims 3 and 4 are cancelled. Claims 2, 5-12 and 19-22 are not amended and remain in the application. Thus, claims 1, 2 and 5-22 are pending in the application. Claims 1 and 14-17 are independent.

Reconsideration of the application and withdrawal of the rejections of the claims are respectfully requested in view of the foregoing amendments and the following remarks.

I. Rejections Under 35 U.S.C. § 103

A. Claims 1, 12-18 and 21-22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Inaba et al. (U.S. Patent No. 5,477,557, hereinafter "Inaba") in view of Kobayashi et al. (U.S. Patent No. 6,181,718, hereinafter "Kobayashi").

Without acquiescing to this rejection, independent claims 1 and 14-17 have each been amended to emphasize additional distinctions over the applied references. Claims 1 and 14-17 have each been amended to include the features of claim 4. As acknowledged by the Office, neither Inaba nor Kobayashi disclose or suggest the features of claim 4.

Claims 3 and 4 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Inaba in view of Kobayashi and Nagarajan (U.S. Patent No. 5,760,939). This rejection is respectfully traversed.

With reference to Figure 1, for example, an exemplary embodiment of the present disclosure provides an optical semiconductor device that includes an optical semiconductor element (e.g., laser diode (LD) 20) having a cathode and an anode. The optical semiconductor device also includes a first conductor line (e.g., lower line extending from the distributed constant circuit 18) connected to the cathode of the optical semiconductor element, and supplying a first electric signal (e.g., positive phase signal) to the optical semiconductor element (e.g., LD 20). The optical semiconductor device also includes a second conductor line (e.g., lower line extending from the distributed constant circuit 18) connected to the anode of the

optical semiconductor element (e.g., LD 20), and supplying a second electric signal (e.g., anti-phase signal) to the optical semiconductor element (e.g., LD 20).

As described beginning at line 2 on page 20 of the original specification, and as illustrated in Figure 1, the optical semiconductor device of the exemplary embodiment also includes a first inductance element (e.g., solenoid 21a) connected to the cathode of the optical semiconductor element (e.g., LD 20) and the first conductor line. In addition, the exemplary optical semiconductor device includes a second inductance element (e.g., solenoid 21b) connected between the anode of the optical semiconductor element (e.g., LD 20) and a ground potential (e.g., the ground potential above the upper horizontal dotted line denoting LD module 2) such that one end of the second inductance element (e.g., solenoid 21b) is connected at the ground potential. The disclosed embodiment provides that the second inductance element (e.g., solenoid 21b) is also connected to the second conductor line.

The optical semiconductor device of the exemplary embodiment also includes a first bias circuit (e.g., bias circuit 28a), which includes the first inductance element (e.g., solenoid 21a) and a first resistor (e.g., resistor 22a) connected in parallel to the first inductance element (e.g., solenoid 21a). In addition, the optical semiconductor device of the exemplary embodiment includes a second bias circuit (e.g., bias circuit 28b), which includes the second inductance element (e.g., solenoid 21b) and a second resistor (e.g., resistor 22b) connected in parallel to the second inductance element (e.g., solenoid 21b). As described in lines 8-10 on page 21 of the specification, for example, the first and second bias circuits act as ungrounded open terminals for high frequencies.

Independent claims 1 and 14-17 recite various features of the above-described exemplary embodiment.

For example, claim 1 recites that the optical semiconductor device comprises an optical semiconductor element which has a cathode and an anode. In addition, claim 1 recites that the optical semiconductor comprises a first inductance element connected to the cathode of the optical semiconductor element and the first conductor line. The optical semiconductor device of claim 1 also comprises a second inductance element which is connected between the anode of the optical semiconductor element and a ground potential such that one end of the second

inductance element is connected at the ground potential, and which is connected to the second inductance element.

In addition, claim 1 recites that the optical semiconductor device comprises a first bias circuit including the first inductance element and a first resistor connected in parallel to the first inductance element. Furthermore, claim 1 recites that the optical semiconductor device comprises a second bias circuit including the second inductance element and a second resistor connected in parallel to the second inductance element.

Independent claims 14-17 each recite an optical semiconductor device with similar features to those described above with respect to claim 1.

With the claimed invention as a road map, the Office proposed to substantially modified Inaba and Kobayashi, and alleged that the hypothetical combination of Inaba and Kobayashi based on Applicants' disclosure would arrive at the arrangement of the optical semiconductor element, first and second conductor lines, and first and first and second inductance elements, as recited in claim 1, as well as the corresponding elements in claims 14-17. Applicants maintain that the Office's hypothetical combination does not result in the arrangement of the optical semiconductor element, first and second conductor lines, and first and first and second inductance elements, as recited in claim 1, as well as the corresponding elements in claims 14-17, for the reasons presented in Applicants' prior response.

Without acquiescing to the rejections of claims 1 and 14-17 based on the Office's hypothetical combination of Inaba and Kobayashi to correspond to Applicant's disclosure, claims 1 and 14-17 have each been amended to include the features of claim 4.

As acknowledged by the Office, Inaba and Kobayashi do not disclose, suggest or even contemplate the first and second bias circuits as recited previously in claim 4 and now recited in claims 1 and 14-17.

In an attempt to arrive at the features of claim 4, the Office proposed to additionally modify Inaba and Kobayashi with Nagarajan, under the apparent belief that it would be have been obvious to arrive at the features of claim 4 merely because Nagarajan discloses a resistor in parallel with an inductor (see Fig. 1). Based on this parallel arrangement, the Office alleged that it "would have been

obvious...to combine the circuit of Inaba [and Kobayashi] with the resistor of Nagarajan in order to adjust the impedance value of the filter and the corresponding filter frequencies.

With reference to Fig. 1, Nagarajan discloses that the transmitter module 10 includes a DC bias circuit 10 in which an inductor and resistor are connected in parallel to the cathode of diode 14.

The Office's reliance on Nagarajan is misplaced and not supportable. Claim 1 recites a first bias circuit and a second bias circuit. In particular, claim 1 recites that the optical semiconductor device comprises a first bias circuit including the first inductance element and a first resistor connected in parallel to the first inductance element, and a second bias circuit including the second inductance element and a second resistor connected in parallel to the second inductance element. Claim 1 recites that the second inductance element is connected between the anode of the optical semiconductor element and a ground potential such that one end of the second inductance element is connected at the ground potential.

Nagarajan does not disclose, suggest or contemplate any arrangement in which an inductor and resistor are connected in parallel to the anode of diode 20.

Furthermore, adding the DC bias circuit 16 of Nagarajan to the combined circuit of Inaba and Kobayashi would defeat the Office's stated motivation for combining Inaba and Kobayashi. The Office asserted that the motivation for combining Inaba and Kobayashi would be to "provide impedance matching to the driving circuit [i.e., transistors Q1 and Q2] and improve the frequency response of the device." However, adding the DC bias circuit 16 of Nagarajan would defeat the purpose of combining Inaba and Kobayashi to provide impedance matching and improved frequency response for any hypothetical second bias circuit on the anode side of the laser diode LD of Inaba or Kobayashi.

Therefore, even with the hypothetical combination of Inaba and Kobayashi proposed by the Office's based on Applicants' disclosure, Nagarajan would not suggest to one skilled in the art to provide a second bias circuit including the second inductance element and a second resistor connected in parallel to the second inductance element, where the second inductance element is connected between

the anode of the optical semiconductor element and a ground potential such that one end of the second inductance element is connected at the ground potential.

Accordingly, Applicants respectfully submit that Nagarajan does not cure the deficiencies of Inaba and Kobayashi for failing to disclose or suggest a second bias circuit including the second inductance element and a second resistor connected in parallel to the second inductance element, where the second inductance element is connected between the anode of the optical semiconductor element and a ground potential such that one end of the second inductance element is connected at the ground potential, as recited in claim 1.

Therefore, Applicants respectfully submit that claim 1 is patentable over Inaba, Kobayashi and Nagarajan, since Inaba, Kobayashi and Nagarajan, either individually or in combination, do not disclose or suggest all the recited features of claim 1.

In addition, Applicants respectfully submit that claims 14-17, which recite a second bias circuit similar to the second bias circuit of claim 1, are also patentable over Inaba, Kobayashi and Nagarajan, for similar reasons to those presented above with respect to claim 1.

Therefore, Applicants respectfully request that claims 1 and 14-17 are patentable over Inaba, Kobayashi and Nagarajan, since one skilled in the art would not have reason or been motivated to combine the references in the manner proposed by the Office.

B. Dependent claims 2, 5, 19 and 20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Inaba and Kobayashi in view of Nagahori, Takeshi et al. ("An Analog Front-End Chip Set Employing an Electro-Optical Mixed Design on SPICE for 5-Gb/s/ch Parallel Optical Interconnection." IEEE Journal of Solid-State Circuits, Volume 36, No. 12, pp 1984-1994, December 2001, hereinafter "Takeshi"). Dependent claim 6 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Inaba, Kobayashi, Takeshi and further in view of Ito et al. (U.S. Patent No. 4,975,664, hereinafter "Ito").

In addition, dependent claims 7-9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Inaba, Kobayashi, Takeshi, Ito and further in view of

Kobayashi et al. (U.S. Patent No. 5,982,793, hereinafter "Kobayashi '793"). Lastly, dependent claims 10-11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Inaba, Kobayashi and further in view of Kobayashi '793.

As discussed above, Inaba, Kobayashi and Nagarajan, either individually or in combination, do not disclose or suggest the recited combination of the optical semiconductor element, first and second conductor lines, first and first and second inductance elements, and first and second bias circuits, as recited in claim 1, as well as their corresponding features in claims 14-17.

Similarly, Takeshi, Ito and Kobayashi '793 also each fail to disclose or suggest the recited combination of the optical semiconductor element, first and second conductor lines, first and first and second inductance elements, and first and second bias circuits, as recited in claim 1, as well as their corresponding features in claims 14-17.

Consequently, Takeshi, Ito and Kobayashi '793 cannot cure the deficiencies of Inaba and Kobayashi for failing to disclose or suggest all the recited features of claims 1 and 14-17.

Accordingly, no obvious combination of Inaba, Kobayashi, Nagarajan, Takeshi, Ito, and Kobayashi '793 can result in the subject matter of claims 1 and 14-17, since these references, either individually or in combination, fail to disclose or suggest all the recited features of claims 1 and 14-17.

Therefore, Applicants respectfully submit that claims 1 and 14-17, as well as claims 2-13 and 18-22 which depend therefrom, are patentable over the applied references.

Dependent claims 2, 5 and 18-22 recite further distinguishing features over the applied references, and are also patentable by virtue of depending from claims 1 and 14-17. The foregoing explanation of the patentability of independent claims 1 and 14-17 is sufficiently clear such that it is believed to be unnecessary to separately demonstrate the additional patentable features of the dependent claims at this time. However, Applicants reserve the right to do should it become appropriate.

II. Conclusion

In view of the foregoing amendments remarks, it is respectfully submitted that the present application is clearly in condition for allowance. Accordingly, favorable examination and consideration of the instant application are respectfully requested.

If, after reviewing this Amendment, the Examiner believes there are any issues remaining which must be resolved before the application can be passed to issue, the Examiner is respectfully requested to contact the undersigned by telephone in order to resolve such issues.

Respectfully submitted,

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Date: September 9, 2010

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